What is claimed is:

[Claim 1] 1. A method of fabricating a dynamic random access memory cell, comprising the steps of:

providing a substrate having a patterned mask layer thereon and a deep trench therein, wherein the patterned mask layer exposes the deep trench, and the substrate has a lower electrode formed at the bottom portion of the deep trench, wherein the interior surface of the deep trench has a capacitor dielectric layer thereon;

filling with a first conductive layer at the bottom portion of the deep trench;

removing the capacitor dielectric layer uncovered by the first conductive layer;

forming a collar oxide layer on the sidewall of the deep trench uncovered by the first conductive layer;

filling with a second conductive layer over the first conductive layer in the deep trench;

forming a trench in the substrate on one side of the second conductive layer, wherein the trench exposes a portion of the substrate and the second conductive layer;

forming a semiconductor strip in the trench to expose a portion of the substrate at the bottom portion of the trench, wherein one end of the semiconductor strip is positioned next to the second conductive layer while the other end of the semiconductor strip is positioned next to the substrate;

forming a gate dielectric layer over the substrate to cover the exposed semiconductor strip and the substrate; and

forming a gate over the gate dielectric layer, wherein the gate crosses over the semiconductor strip, and the gate-covered portion of the semiconductor strip serves as a channel region.

[Claim 2] 2. The method according to claim 1, wherein the semiconductor strip comprises epitaxial silicon.

[Claim 3] 3. The method according to claim 1, wherein the step for forming the semiconductor strip comprises:

depositing a semiconductor material layer into the trench; and patterning the semiconductor material layer.

[Claim 4] 4. The method according to claim 3, wherein the step of patterning the semiconductor material layer further comprises removing a portion of the patterned mask layer and the substrate.

[Claim 5] 5. The method according to claim 1, wherein the step of forming the semiconductor strip in the trench further comprises forming a first extension portion and a second extension portion on each end of the semiconductor strip so that an H-shaped semiconductor layer is formed.

[Claim 6] 6. The method according to claim 1, further comprising forming a doped region in a portion of the semiconductor strip adjacent to the substrate and in the substrate adjacent to the semiconductor strip after forming the gate.

[Claim 7] 7. The method according to claim 1, wherein the step of forming the collar oxide layer comprises:

forming a collar oxide material layer on the sidewall of the deep trench, the top of the first conductive layer and the substrate; and

removing the collar oxide material layer on the top of the first conductive layer and the substrate.

[Claim 8] 8. The method according to claim 1, further comprising forming a doped stripe in the substrate adjacent to the lower electrode before forming the trench in the substrate on one side of the second conductive layer.

[Claim 9] 9. The method according to claim 1, further comprising forming a doped well in a portion of the second conductive layer and the substrate before forming the trench in the substrate on one side of the second conductive layer, so that the trench is formed within the doped well.

[Claim 10] 10. A method of fabricating a dynamic random access memory cell, comprising the steps of:

providing a substrate having a patterned mask layer thereon and a deep trench capacitor therein, wherein the deep trench capacitor comprises a

lower electrode, an upper electrode, a capacitor dielectric layer and a collar oxide layer, and the patterned mask layer exposes the upper electrode;

forming a trench in the substrate on one side of the deep trench capacitor, wherein the trench exposes a portion of the substrate and the upper electrode;

depositing a semiconductor material layer into the trench;

patterning the semiconductor material layer to form a semiconductor strip and two openings exposing the substrate, wherein one end of the semiconductor strip is positioned next to the upper electrode while the other end of the semiconductor strip is positioned next to the substrate;

forming a gate dielectric layer over the substrate to cover the exposed semiconductor strip and the substrate; and

forming a conductive layer over the gate dielectric layer, wherein the conductive layer crosses over the semiconductor strip, and the semiconductor strip covered by the conductive layer serves as a channel region.

[Claim 11] 11. The method according to claim 10, wherein the semiconductor strip comprises epitaxial silicon.

[Claim 12] 12. The method according to claim 10, wherein the step of forming the semiconductor strip in the trench further comprises forming a first extension portion and a second extension portion on each end of the semiconductor strip so that an H-shaped semiconductor layer is formed.

[Claim 13] 13. The method according to claim 10, further comprising forming a doped region in a portion of the semiconductor strip adjacent to the substrate and in the substrate adjacent to the semiconductor strip after forming the conductive layer.

[Claim 14] 14. The method according to claim 10, wherein the step of patterning the semiconductor material layer further comprises removing a portion of the patterned mask layer and the substrate.

[Claim 15] 15. The method according to claim 10, wherein the upper electrode comprises a first conductive layer and a second conductive layer, and the semiconductor strip is positioned next to the second conductive layer.

[Claim 16] 16. The method according to claim 15, further comprising forming a doped well in a portion of the second conductive layer and the substrate before forming the trench in the substrate on one side of the deep trench capacitor, so that the trench is formed within the doped well.

[Claim 17] 17. The method according to claim 10, further comprising forming a doped stripe in the substrate adjacent to the lower electrode before forming the trench in the substrate on one side of the deep trench capacitor.

[Claim 18] 18. A dynamic random access memory cell, comprising:

a deep trench capacitor disposed inside a deep trench in a substrate, wherein the deep trench capacitor further comprises:

a lower electrode disposed in the substrate at a bottom portion of the deep trench;

an upper electrode disposed within the deep trench;

a capacitor dielectric layer disposed between the bottom portion of the deep trench and the upper electrode; and

a collar oxide layer disposed on the sidewall of the deep trench exposed by the capacitor dielectric layer and disposed between the upper electrode and the substrate; and

an active device disposed inside a trench in the substrate, wherein the active device is positioned next to the deep trench capacitor, wherein the active device further comprises:

a semiconductor strip disposed inside the trench to expose a portion of the substrate at the bottom portion of the trench, wherein one end of the semiconductor strip is positioned next to the substrate while the other end of the semiconductor strip is positioned next to the upper electrode;

a gate dielectric layer disposed on the semiconductor strip;

a gate disposed on the gate dielectric layer, wherein the gate crosses over the semiconductor strip, and the semiconductor strip covered by the gate serves as a channel region; and

a doped region disposed in a portion of the semiconductor strip adjacent to the substrate and in the substrate adjacent to the semiconductor strip.

[Claim 19] 19. The dynamic random access memory cell according to claim 18, wherein the semiconductor strip comprises epitaxial silicon.

[Claim 20] 20. The dynamic random access memory cell according to claim 18, wherein the semiconductor strip further comprises a first extension portion and a second extension portion respectively attached to each end of the semiconductor strip so that an H-shaped semiconductor layer is formed.

[Claim 21] 21. The dynamic random access memory cell according to claim 18, wherein the upper electrode comprises a first conductive layer and a second conductive layer, the capacitor dielectric layer is disposed between the bottom portion of the deep trench and the first conductive layer, the collar oxide layer is disposed between the second conductive layer and the substrate, and the semiconductor strip is positioned next to the second conductive layer.

[Claim 22] 22. The dynamic random access memory cell according to claim 18, further comprising a doped stripe disposed in the substrate adjacent to the lower electrode of the deep trench capacitor.

[Claim 23] 23. The dynamic random access memory cell according to claim 18, further comprising a doped well such that the trench is disposed inside the doped well.